BIOS Writer's Guide:

iDRAGON™ mP6 IA PROCESSOR

A Key Innovation for Information Appliances

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Introduction

The Rise™ *iDragon™mP6:* the IA processor is a sixth generation processor optimized for low power consumption, high-performance information appliance applications. The innovative Rise™ *iDragon™ mP6* IA processor is the first superscalar, superpipelined, Pentium® MMX* compatible processor featuring 3 integer units, 3–way superscalar MMX technology, and a fully pipelined floating point unit. The innovative circuitry of the Rise™ *iDragon™ mP6* IA processor gives the users the utmost multimedia performance, maximizes processing per clock cycle while requiring minimal power consumption – providing an ideal choice for thermal efficient set-top box, internet box, thin client and home gateway etc.

This document is intended for BIOS and operating system software developers and contains information required to implement system support for the Rise™ *iDragon™ mP6* IA processor.

CPUID

The CPUID instruction should be used to detect the Rise™ *iDragon™ mP6* IA processor and the model–specific features supported. Unsupported features should not be used by the BIOS, operating system, or by the application software. The Rise™ *iDragon™ mP6* IA processor returns values for the CPUID instruction are shown in Tables 1 through 3. The Intel P55C processor return values are included in the tables for comparison.

When the BIOS identifies the processor, if the processor is a Rise™

its name should appear as “Rise(tm) iDragon (tm) *mP6*–xxxMIPS”

– Where xxx is the rated performance number (refer to Table 4).

TABLE 1. CPUID RETURN VALUES WITH EAX == 0

REGISTER	*iDragon™ mP6*	P55C
EAX	1	1
EBX:ECX:EDX	RiseRiseRise	GenuineIntel

TABLE 2. CPUID EAX RETURN VALUES WITH EAX == 1

PROCESSOR	[13:12] Type ID	[11:8] Family ID	[7:4] Model ID	[3:0] Stepping ID
iDragon™ mP6	0	5	2	Varies
P55C	0	5	4	Varies

TABLE 3. CPUID EDX RETURN VALUES WITH EAX == 1

EDX Bits — Meaning	*iDRAGON™ mP6*	P55C	Notes
0 — Floating Point Unit on Chip (FPU)	1	1	
1 — VM86 Extensions (VME)	0	1	
2 — Debugging Extensions (DE)	0	1	
3 — Page Size Extensions (PSE)	0	0	
4 — Time Stamp Counter (TSC)	1	1	
5 — Model Specific Registers (MSR)	0	1	
6 — Physical Address Extensions (PAE)	0	0	
7 — Machine Check Exception (MCE)	0	1	
8 — CMPXCHG8B instruction (CX8)	0	1	1
9 — APIC supported	0	1	2
10:11 — RESERVED	-	-	
12 — Memory Type Range Registers (MTRR)	0	0	
13 — PTE Global Flag (PGE)	0	0	
14 — Machine Check Architecture (MCA)	0	0	
15 — Conditional Move supported (CMOV)	0	0	
16:22 — RESERVED	-	-	
23 — MMX* supported	1	1	
24:31 — RESERVED	-	-	

Notes:

1. The CMPXCHG8B instruction is supported and always enabled on the Rise™ *iDragon™ mP6* IA processor; however, as specified in an erratum for early versions of Windows NT* 4.0, the default CPUID function bit is set to 0.
2. Pentium processor multiprocessing capabilities are not supported on the Rise™ *iDragon™ mP6* IA processor.

CPU Speed Detection

The Rise™ *iDragon™ mP6* IA processor supports the Time Stamp Counter and the RDTSC instruction. BIOS algorithms may use this facility to measure timed operations for Processor speed detection. During system boot, BIOS detects and displays the speed/ratio for the processor.

CPU Core Speed Rating

A lookup table that references the processor operating frequency to a performance rating number should be incorporated into the speed detection algorithm. Tables 4 is the performance lookup table for *iDragon™ mP6* IA processor.

TABLE 4. *iDragon*™ mP6 PERFORMANCE RATING LOOKUP TABLE

Bus Speed	Bus Ratio	Performance Rating
100	2:1	500 MIPS
100	2.5:1	600 MIPS

Version / Stepping Specific Configuration

For the production version of the Rise™ *iDragon*™ *mP6* IA processor, no stepping–specific initialization is required.

Control Register CR4

The Pentium® processor introduced a new control register (CR4) for controlling many of its new model–specific architectural features. The Rise™ *iDragon*™ *mP6* IA processor provides a CR4 register compatible with the Pentium processor; however, it does not implement all of the model–specific features that can be controlled through the CR4 register. The CPUID instruction described in Section 0 should be used to determine the features supported by the Rise™ *iDragon*™ *mP6* IA processor.

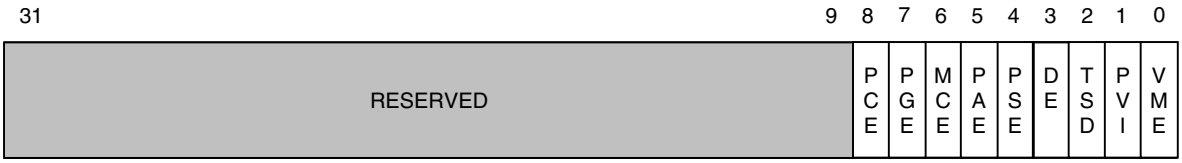

Figure 1. Control Register CR4 Bit Assignments

Bits **VME, PVI, PSE, MCE, PGE** and **PCE** are not supported on the Rise™ *iDragon*™ *mP6* IA processor. These six bits return a value of 0 when read and although they cannot be set, no GP exception occurs on attempts to set them.

The **DE** bit is reserved on the Rise™ *iDragon*™ *mP6* IA processor. The return value when this bit is read and its response to attempts to set it are both undefined; however, no GP exception occurs on attempts to set or clear it.

iDragon™ *mP6* IA Processor Reset and Init States

The state of each register of the *iDragon*™ *mP6* IA processor after a RESET or INIT is listed in Table 5.

TABLE 5. *iDragon™ MP6* IA PROCESSOR PARCHITECTURAL STATE AFTER RESET OR INIT

REGISTER	RESET State	INIT State[1]	NOTES
EFLAGS	00000002H		2
EIP	0000FFF0H		
CS	Selector = F000H Base = FFFF0000H Limit = FFFFH AR = Present, R/W, Accessed		
SS, DS, ES, FS, GS	Selector = 0000H Base = 00000000H Limit = FFFFH AR = Present, R/W, Accessed		
EAX	00000000H		3
EDX	0000050xH		4
EBX, ECX, ESI, EDI, EBP, ESP	00000000H		
GDTR, IDTR	Base = 00000000H Limit = FFFFH AR = Present, R/W		
LDTR, Task Register	Selector = 0000H Base = 00000000H Limit = FFFFH AR = Present, R/W		
FPU Stack ST7-ST0	00000000000000000000H (+0.0)	Unchanged	
FPU Control Word	0040H	Unchanged	
FPU Status Word	0000H	Unchanged	
FPU Tag Word	5555H	Unchanged	
FPU Instruction Pointer	000000000000H	Unchanged	
FPU Data Pointer	000000000000H	Unchanged	
CR0	60000010H		5
CR2, CR3, CR4	00000000H		
DR7	00000400H		
DR6	FFFF0FF0H		
DR0, DR1, DR2, DR3	00000000H		
Data and Code Cache	Invalid	Unchanged	
TLBs	Invalid	Invalid	
TSC	0	Unchanged	

Notes:

1. Unless otherwise specified, the INIT state is the same as the RESET state.
2. Software should not depend on the states of the 10 most significant bits of the EFLAGS register following a reset.
3. The EAX register contains the results of the Built In Self Test (BIST) when invoked. If EAX = 00000000H then BIST completed successfully. If EAX is non-zero then BIST failed.
4. The EDX register contains the Rise™ *iDragon™ mP6* IA processor identification and revision information.
5. The CD and NW flags are unchanged following INIT, bit 4 is set to 1, and all other bits are cleared.

System Management Mode

The System Management Mode (SMM) of the Rise™ *iDragon™ mP6* IA processor is functionally identical to that of the Pentium® processor. SMM handlers should not rely on the availability of any Pentium processor model–specific registers or features that are not supported by the Rise™ *iDragon™ mP6* IA processor. The CPUID instruction should be used to determine the model–specific features available.

8.1 SMM State–Save Area

When the Rise™ *iDragon™ mP6* IA processor enters SMM, it writes the processor state information into the SMM state–save area of SMRAM. The SMM state–save map area is located in SMRAM between addresses [SMBASE + 8000H + 7FFFH] and [SMBASE + 8000H + 7E00H]. Table 6 lists the information contained within the SMM state–save area. Processor state information not listed in Table 6 is not automatically saved nor restored by the processor. It is the responsibility of the SMM handler to save and restore any additional state information that it alters during execution.

TABLE 6. SMM STATE–SAVE AREA MAP

OFFSET (Added to SMBASE + 8000H)	REGISTER	WRITABLE
7FFCH	CR0	No
7FF8H	CR3	No
7FF4H	EFLAGS	Yes
7FF0H	EIP	Yes
7FECH	EDI	Yes
7FE8H	ESI	Yes
7FE4H	EBP	Yes
7FE0H	ESP	Yes
7FDCH	EBX	Yes
7FD8H	EDX	Yes
7FD4H	ECX	Yes
7FD0H	EAX	Yes
7FCCH	DR6	No
7FC8H	DR7	No
7FC4H	TR	No

OFFSET (Added to SMBASE + 8000H)	REGISTER	WRITABLE
7FC0H	LDTR Base	No
7FBCH	GS	No
7FB8H	FS	No
7FB4H	DS	No
7FB0H	SS	No
7FACH	CS	No
7FA8H	ES	No
7FA7H – 7F98H	RESERVED	No
7F94H	IDT Base	No
7F92H	IDT Limit (Word)	No
7F91H – 7F8CH	RESERVED	No
7F88H	GDT Base	No
7F86H	GDT Limit (Word)	No
7F85H – 7F04H	RESERVED	No
7F02H	Auto HALT Restart Field (Word)	Yes
7F00H	I/O Instruction Restart Field (Word)	Yes
7EFCH	SMM Revision Identifier Field	No
7EF8H	SMBASE Field	Yes
7EF7H – 7EF4H	RESERVED	No
7EF0H	Restart EIP	No
7EEFH – 7EE8H	RESERVED	No
7EE4H	CR4	No
7EE0H	CR2	No
7ED8H	TSS Descriptor	No
7ED0H	LDT Descriptor	No
7EC8H	GS Descriptor	No
7EC0H	FS Descriptor	No
7EB8H	DS Descriptor	No
7EB0H	SS Descriptor	No
7EA8H	CS Descriptor	No
7EA0H	ES Descriptor	No
7E9FH – 7E00H	RESERVED	No

8.2 SMM Initial Register Values

The initial state of each processor register upon entry to SMM is listed in Table 7.

TABLE 7. REGISTER INITIALIZATION IN SMM

REGISTER	INITIAL CONTENTS	NOTES
General-purpose registers	Undefined	
EFLAGS	00000002H	
EIP	00008000H	
CS Selector	SMM Base shifted right 4 bits (default 3000H)	1
CS Base	SMM Base (default 00030000H)	1
CS Limit	FFFFFH (4 GBytes)	1
DS, ES, FS, GS, SS Selectors	0000H	1
DS, ES, FS, GS, SS Bases	00000000H	1
DS, ES, FS, GS, SS Limits	FFFFFH (4 GBytes)	1
CR0	Bits 0, 2, 3 and 31 are cleared; others unmodified	
DR6	Unpredictable	
DR7	00000400H	

Notes:

1. Attr=Preset. R/W. Accessed, G=1, D=0, AVL=0, DPL=0

8.3 SMM Revision Identifier

The SMM Revision Identifier is used to ascertain the version and extensions of SMM being used and is located at offset 7EFCH in the SMM state–save area. Table 8 shows the SMM Revision Identifier Fields and associated Rise™ *iDragon*™ *mP6* IA processor default values. I/O Instruction Restart and SMBase Relocation are always enabled on the Rise™ *iDragon*™ *mP6* IA processor.

TABLE 8. SMM REVISION IDENTIFIER FIELDS

BITS 31-18	BIT 17	BIT 16	BITS 15-0
RESERVED	SMM Base Relocation	I/O Instruction Restart	SMM Revision Level
0	1	1	0002H

8.4 I/O Instruction Restart

The I/O Instruction Restart Field, located at offset 7F00H in the SMM state–save area, controls an I/O instruction restart. If the I/O Instruction Restart Field contains the value 00FFH during an RSM instruction, then the value restored in the EIP register is the value found in the Restart EIP Field of the SMM state–save area. This restored EIP points to the I/O instruction that received the SMI request, and the processor automatically re–executes the trapped I/O instruction. However, if the I/O Instruction Restart Field contains the value 0000H during an RSM instruction, then the value restored in the EIP register is located in the EIP Field in the SMM state–save area. This information is tabulated below.

Value of I/O Instruction Field	Origin of Value Stored in EIP Register
00FFh	Restart EIP Field of SMM State–Save Area
0000H	EIP Register Field of SMM State–Save Area

I/O Instruction Restart is always enabled on the Rise™ *iDragon*™ *mP6* IA processor. When the processor enters SMM, a value of 0000H is always written to the I/O Instruction Restart Field. It is the responsibility of the SMM handler to examine the state of the processor and to determine if an I/O instruction restart is required.

8.5 Auto Halt Restart

The Auto Halt Restart Field, located at offset 7F02H in the SMM state–save area, is loaded with a value of 0001H if the processor was in the HALT state when the SMI occurred. If the processor was not in HALT state, a value of 0000H is saved. Upon exit of SMM, the processor examines the Auto Halt Restart Field. If the Auto Halt Restart Field contains a value of 0001H, the Restart EIP is restored to the EIP register and the processor re–executes the HALT instruction upon exit of SMM. However, if the Auto Halt Restart Field contains 0000H, then the value from the EIP field is restored to the EIP register and the processor begins execution at the instruction following the HALT. If the SMM Handler routine clears this flag, the processor begins execution with the instruction following the HALT instruction.

8.6 Back–to–Back SMI Interrupts When Using I/O Instruction Restart

To avoid program error, the SMM handler must be able to identify back–to–back SMI interrupts on I/O instructions when I/O Instruction Restarting is being used. Setting the I/O Instruction Restart Field value to 00FFH during the second of the back–to–back executions of the SMM handler causes the EIP value to be set.

Appendix A – Machine–Specific Code for Rise™ *iDragon*™ *mP6* Configuration Setting

The following code should be included in the system BIOS to properly support feature validation of the production steppings of the Rise™ *iDragon*™ *mP6* IA processor. Include it in the non–compressed area so that it is available to vendors for easy modification to facilitate validation of different bit settings.

```
;*************************************************************************
;Routine:   mP6_Msr_Setup_Reg
;
;Purpose:   For configuration setup of iDragon mP6 IA Processor
;
;Comment:   This routine should be used to do configuration setup on iDragon
;
;Inputs:    None
;
;Outputs:   None
;*************************************************************************

Public   mP6_Msr_Setup_Reg

mP6_Msr_Setup_Reg Proc  Near

      pushad
      mov      eax, 6363452Ah
      mov      ecx, 3231206Ch
      mov      edx, 2A32313Ah
      cpuid

      mov      eax, 63634523h
      mov      ecx, 32315F6Ch
      mov      edx, 2333313Ah
      cpuid

      popad
      ret

mP6_Msr_Setup_Reg endp
```